CS5368

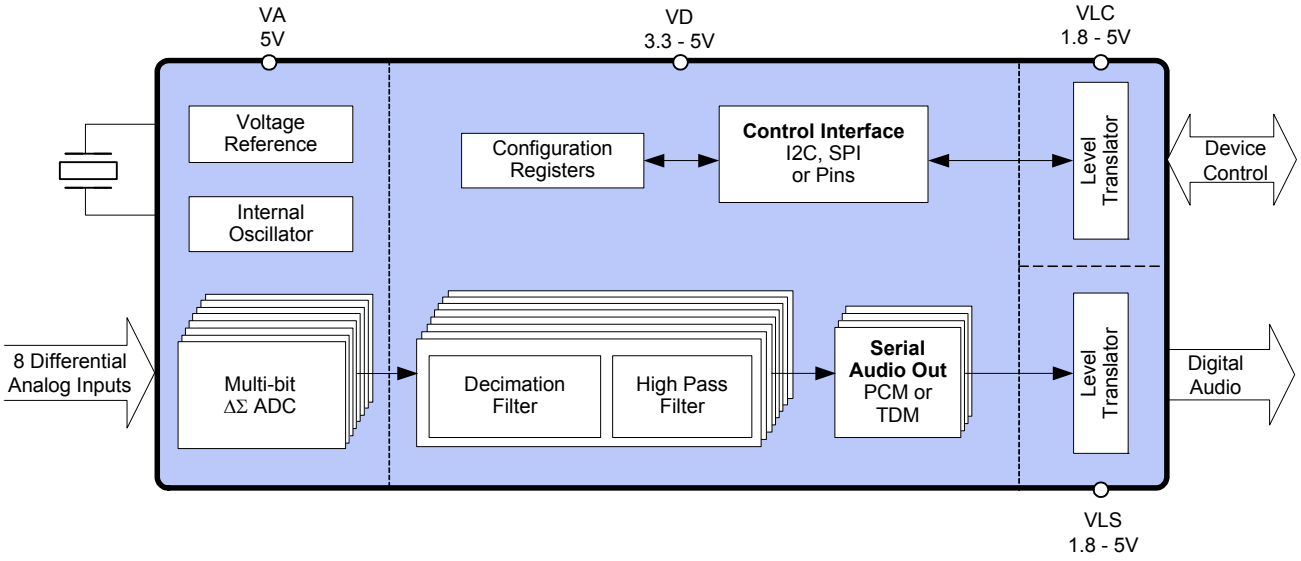
114 dB, 192 kHz, 8-Channel A/D Converter

Features

- Advanced Multi-bit Delta-Sigma Architecture
- 24-Bit Conversion
- 114 dB Dynamic Range
- -105 dB THD+N
- Supports Audio Sample Rates up to 216 kHz
- Selectable Audio Interface Formats
  - Left-Justified, I²S, TDM
  - 8-Channel TDM Interface Formats
- Low Latency Digital Filter
- Less than 680 mW Power Consumption
- On-Chip Oscillator Driver
- Operation as System Clock Master or Slave
- Auto-Detect Speed in Slave Mode
- Differential Analog Architecture
- Separate 1.8 V to 5 V Logic Supplies for Control and Serial Ports
- High-Pass Filter for DC Offset Calibration
- Overflow Detection
- Footprint Compatible with the 4-Channel CS5364 and 6-Channel CS5366

Additional Control Port Features

- Supports I²C or SPI™ Control Interface per specifications on page 17 and page 18
- Individual Channel HPF Disable
- Overflow Detection for Individual Channels
- Mute Control for Individual Channels
- Independent Power-Down Control per Channel Pair



Description

The CS5368 is a complete 8-channel analog-to-digital converter for digital audio systems. It performs sampling, analog-to-digital conversion, and anti-alias filtering, generating 24-bit values for all 8-channel inputs in serial form at sample rates up to 216 kHz per channel.

The CS5368 uses a 5th-order, multi-bit delta sigma modulator followed by low latency digital filtering and decimation, which removes the need for an external anti-aliasing filter. The ADC uses a differential input architecture which provides excellent noise rejection.

Dedicated level translators for the Serial Port and Control Port allow seamless interfacing between the CS5368 and other devices operating over a wide range of logic levels. In addition, an on-chip oscillator driver provides clocking flexibility and simplifies design.

The CS5368 is the industry's first audio A/D to support a high-speed TDM interface which provides a serial output of 8 channels of audio data with sample rates up to 216 kHz within a single data stream. It further reduces layout complexity and relieves input/output constraints in digital signal processors.

The CS5368 is available in a 48-pin LQFP package in both Commercial (-40°C to 85°C) and Automotive grades (-40°C to +105°C). The CDB5368 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please see "Ordering Information" on page 41 for complete ordering information.

The CS5368 is ideal for high-end and pro-audio systems requiring unrivaled sound quality, transparent conversion, wide dynamic range and negligible distortion, such as A/V receivers, digital mixing consoles, multi-channel recorders, outboard converters, digital effect processors, and automotive audio systems.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. PIN DESCRIPTION

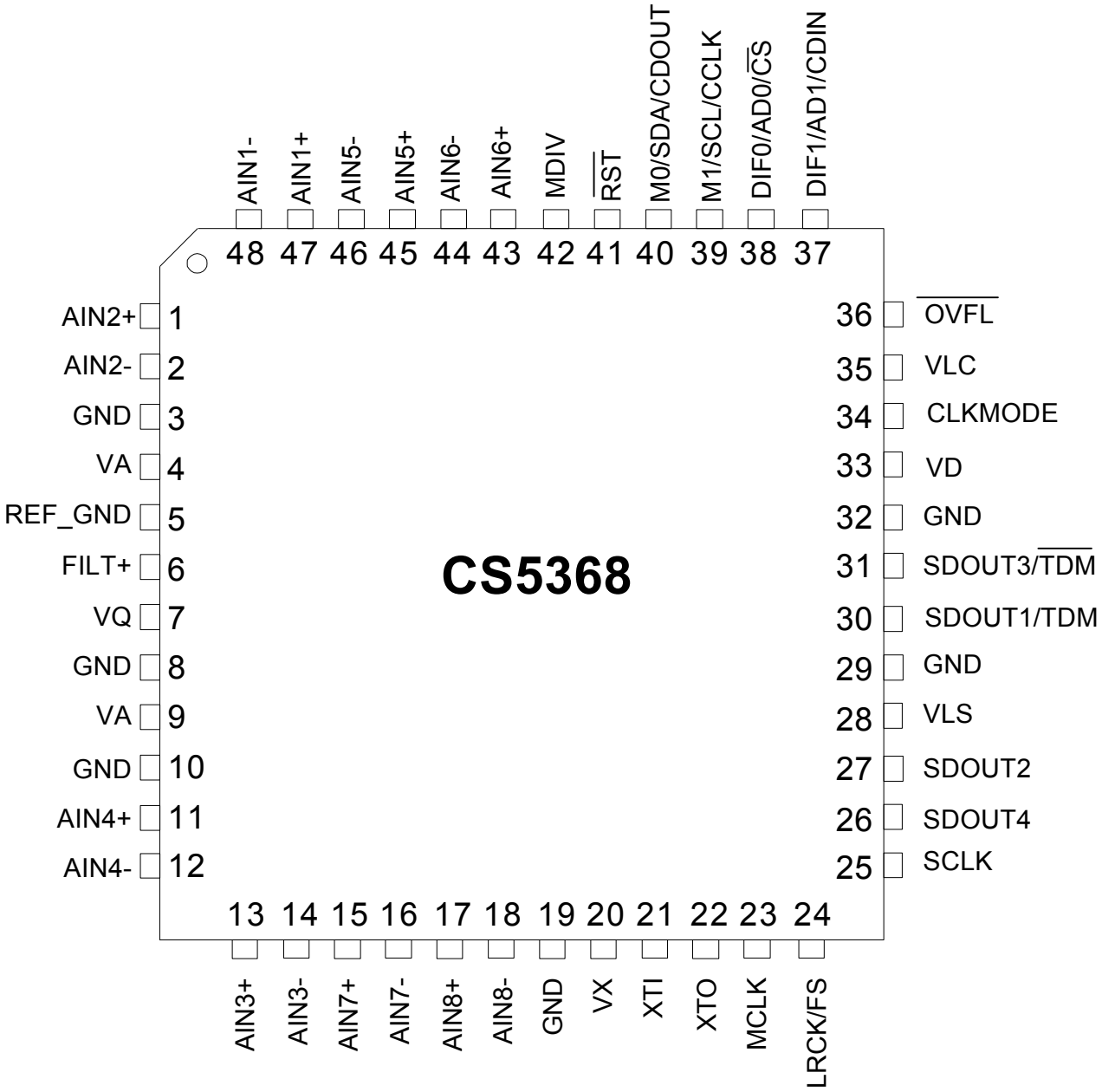


Figure 1. CS5368 Pinout

Pin Name	Pin #	Pin Description
AIN2+, AIN2- AIN4+, AIN4- AIN3+, AIN3- AIN7+, AIN7- AIN8+, AIN8- AIN6+, AIN6- AIN5+, AIN5- AIN1+, AIN1-	1,2 11,12 13,14 15,16 17,18 43,44 45,46 47,48	**Differential Analog** (*Inputs*) - Audio signals are presented differently to the delta sigma modulators via the AIN+/- pins.
GND	3,8 10,19 29,32	**Ground** (*Input*) - Ground reference. Must be connected to analog ground.
VA	4,9	**Analog Power** (*Input*) - Positive power supply for the analog section
REF_GND	5	**Reference Ground** (*Input*) - For the internal sampling circuits. Must be connected to analog ground.
FILT+	6	**Positive Voltage Reference** (*Output*) - Reference voltage for internal sampling circuits.
VQ	7	**Quiescent Voltage** (*Output*) - Filter connection for the internal quiescent reference voltage.
VX	20	**Crystal Oscillator Power** (*Input*) - Also powers control logic to enable or disable oscillator circuits.
XTI XTO	21 22	**Crystal Oscillator Connections** (*Input/Output*) - I/O pins for an external crystal which may be used to generate MCLK.
MCLK	23	**System Master Clock** (*Input/Output*) - When a crystal is used, this pin acts as a buffered MCLK Source (Output). When the oscillator function is not used, this pin acts as an input for the system master clock. In this case, the XTI and XTO pins must be tied low.
LRCK/FS	24	**Serial Audio Channel Clock** (*Input/Output*) In I²S Mode, Serial Audio Channel Select. When low, the odd channels are selected. In LJ Mode, Serial Audio Channel Select. When high, the odd channels are selected. In TDM Mode, a frame sync signal. When high, it marks the beginning of a new frame of serial audio samples. In Slave Mode, this pin acts as an input pin.
SCLK	25	**Main timing clock for the Serial Audio Interface** (*Input/Output*) - During Master Mode, this pin acts as an output, and during Slave Mode it acts as an input pin.
SDOUT4	26	**Serial Audio Data** (*Output*) - Channels 7,8.
SDOUT2	27	**Serial Audio Data** (*Output*) - Channels 3,4.
VLS	28	**Serial Audio Interface Power** (*Input*) - Positive power for the serial audio interface.
SDOUT1/TDM	30	**Serial Audio Data** (*Output*) - Channels 1,2.
SDOUT3/$\overline{\text{TDM}}$	31	**Serial Audio Data** (*Output*) - Channels 5,6. $\overline{\text{TDM}}$ is complementary TDM data.
VD	33	**Digital Power** (*Input*) - Positive power supply for the digital section.
VLC	35	**Control Port Interface Power**(*Input*) - Positive power for the control port interface.
$\overline{\text{OVFL}}$	36	**Overflow** (*Output, open drain*) - Detects an overflow condition on both left and right channels.
$\overline{\text{RST}}$	41	**Reset** (*Input*) - The device enters a low power mode when low.
Stand-Alone Mode		
CLKMODE	34	**CLKMODE** (*Input)* - Setting this pin HIGH places a divide-by-1.5 circuit in the MCLK path to the core device circuitry.
DIF1 DIF0	37 38	**DIF1, DIF0** (*Input*) - Inputs of the audio interface format.
M1 M0	39 40	**Mode Selection** (*Input*) - Determines the operational mode of the device.
MDIV	42	**MCLK Divider** (*Input*) - Setting this pin HIGH places a divide-by-2 circuit in the MCLK path to the core device circuitry.

Control Port Mode		
CLKMODE	34	**CLKMODE** (*Input*) - This pin is ignored in Control Port Mode and the same functionality is obtained from the corresponding bit in the Global Control Register. **Note:** Should be connected to GND when using the part in Control Port Mode.
AD1/CDIN	37	**I²C Format, AD1** (*Input*) - Forms the device address input AD[1]. **SPI Format, CDIN** (*Input*) - Becomes the input data pin.
AD0/$\overline{CS}$	38	**I²C Format, AD0** (*Input*) - Forms the device address input AD[0]. **SPI Format, CS** (Input) - Acts as the active low chip select input.
SCL/CCLK	39	**I²C Format, SCL** (*Input*) – Serial clock for the serial control port. An external pull-up resistor is required for I²C control port operation. **SPI Format, CCLK** (*Input*) – Serial clock for the serial control port.
SDA/CDOUT	40	**I²C Format SDA** (*Input/Output*) - Acts as an input/output data pin. An external pull-up resistor is required for I²C control port operation. **SPI Format CDOUT** (*Output*) - Acts as an output only data pin.
MDIV	42	**MCLK Divider** (*Input*) - This pin is ignored in Control Port Mode and the same functionality is obtained from the corresponding bit in the Global Control Register. **Note:** Should be connected to GND when using the part in Control Port Mode.

2. TYPICAL CONNECTION DIAGRAM

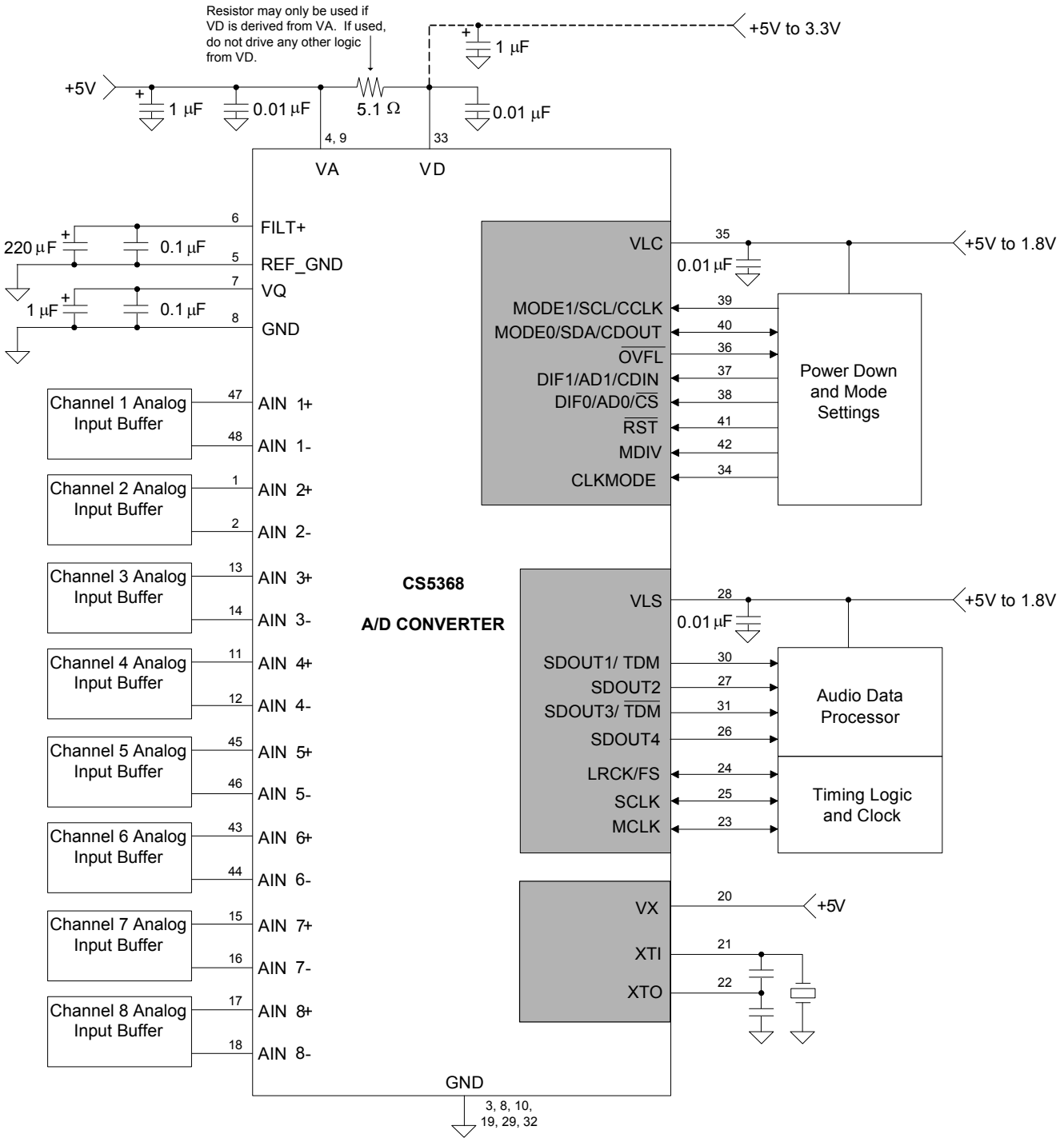


Figure 2. Typical Connection Diagram

For analog buffer configurations, refer to Cirrus Application Note AN241. Also, a low-cost single-ended-to-differential solution is provided on the Customer Evaluation Board.

3. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

GND = 0 V, all voltages with respect to 0 V.

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies:	Positive Analog	VA	4.75	5.0		
	Positive Crystal	VX	4.75	5.0		
	Positive Digital	VD	3.14	3.3	5.25	V
	Positive Serial Logic	VLS	1.71[1]	3.3		
	Positive Control Logic	VLC	1.71	3.3		
Ambient Operating Temperature	(-CQZ)	T_{AC}	-40	-	85	°C
	(-DQZ)	T_{AA}	-40	-	105	

1. TDM Quad-Speed Mode specified to operate correctly at VLS ≥ 3.14 V.

ABSOLUTE RATINGS

Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes. Transient currents up to ±100 mA on the analog input pins will not cause SCR latch-up.

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Analog	VA				
	Positive Crystal	VX				
	Positive Digital	VD	-0.3	-	+6.0	V
	Positive Serial Logic	VLS				
	Positive Control Logic	VLC				
Input Current		I_{in}	-10		+10	mA
Analog Input Voltage		V_{IN}	-0.3		VA+0.3	V
Digital Input Voltage		V_{IND}		-	VL+0.3	
Ambient Operating Temperature (Power Applied)		T_A	-50		+125	°C
Storage Temperature		T_{stg}	-65		+150	

SYSTEM CLOCKING

Parameter	Symbol	Min	Typ	Max	Unit
Input Master Clock Frequency	MCLK	0.512		55.05	MHz
Input Master Clock Duty Cycle	t_{clkhl}	40		60	%

DC POWER

MCLK = 12.288 MHz; Master Mode; GND = 0 V.

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply Current	VA = 5 V	I_A	-	100	112	mA
(Normal Operation)	VX = 5 V	I_X		4	8	
	VD = 5 V	I_D		70	88	
	VD = 3.3 V	I_D		42	50	
	VLS, VLC = 5 V	I_L		12	15	
	VLS, VLC = 3.3 V	I_L		5	8	
Power Supply Current	VA = VX = 5 V	I_A	-	50	-	µA
(Power-Down) (Note 1)	VLS, VLC, VD = 5 V	I_{D+L}		500		
Power Consumption						
Normal Operation	All Supplies = 5 V	-	-	930	1115	mW
	VA = VX = 5 V, VD = VLS = VLC = 3.3 V			675	792	
(Power-Down) (Note 1)				2.75	-	

1. Power-Down is defined as $\overline{RST}$ = LOW with all clocks and data lines held static at a valid logic level.

LOGIC LEVELS

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	%VLS/VLC	V_{IH}	70	-	-	%
Low-Level Input Voltage	%VLS/VLC	V_{IL}	-	-	30	%
High-Level Output Voltage at 100 µA load	%VLS/VLC	V_{OH}	85	-	-	%
Low-Level Output Voltage at -100 µA load	%VLS/VLC	V_{OL}	-	-	15	%
SDA Low-Level Output Voltage at -2 mA load	%VLC	V_{OL}	-	-	TBD	%
$\overline{OVFL}$ Current Sink				-4		mA
Input Leakage Current	logic pins only	I_{in}	-10	-	10	µA

PSRR, VQ AND FILT+ CHARACTERISTICS

MCLK = 12.288 MHz; Master Mode. Valid with the recommended capacitor values on FILT+ and VQ as shown in the “Typical Connection Diagram”.

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Rejection Ratio at (1 kHz)	PSRR	-	65	-	dB
V_Q Nominal Voltage		-	VA/2	-	V
Output Impedance			25		kΩ
Maximum allowable DC current source/sink			10		µA
Filt+ Nominal Voltage		-	VA	-	V
Output Impedance			4.4		kΩ
Maximum allowable DC current source/sink			10		µA

ANALOG CHARACTERISTICS (COMMERCIAL)

Test Conditions (unless otherwise specified). VA = 5 V, VD = VLS = VLC 3.3 V, and T_A = 25° C. Full-scale input sine wave. Measurement Bandwidth is 10 Hz to 20 kHz.

Parameter		Symbol	Min	Typ	Max	Unit
Single-Speed Mode Fs = 48 kHz						
Dynamic Range	A-weighted		108	114	-	dB
	unweighted		105	111	-	
Total Harmonic Distortion + Noise	-1 dB			-105	-99	
referred to typical full scale	-20 dB	THD+N	-	-91	-	dB
	-60 dB			-51	-45	
Double-Speed Mode Fs = 96 kHz						
Dynamic Range	A-weighted		108	114		
	unweighted		105	111	-	dB
	40 kHz bandwidth unweighted		-	108		
Total Harmonic Distortion + Noise	-1 dB			-105	-99	
referred to typical full scale	-20 dB	THD+N	-	-91	-	dB
	-60 dB			-51	-45	
	40 kHz bandwidth -1dB			-102	-	
Quad-Speed Mode Fs = 192 kHz						
Dynamic Range	A-weighted		108	114		
	unweighted		105	111	-	dB
	40 kHz bandwidth unweighted		-	108		
Total Harmonic Distortion + Noise	-1 dB			-105	-99	
referred to typical full scale	-20 dB	THD+N	-	-91	-	dB
	-60 dB			-51	-45	
	40 kHz bandwidth -1dB			-102	-	
Dynamic Performance for All Modes						
Interchannel Isolation			-	110	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Error			-5	-	5	%
Gain Drift			-	± 100	-	ppm/°C
Offset Error	HPF enabled		0	-	-	LSB
	HPF disabled		-	-	100	
Analog Input Characteristics						
Full-scale Differential Input Voltage			1.07*VA	1.13*VA	1.19*VA	Vpp
Input Impedance (Differential)			-	250	-	kΩ
Common Mode Rejection Ratio		CMRR	-	82	-	dB

ANALOG CHARACTERISTICS (AUTOMOTIVE)

Test Conditions (unless otherwise specified). VA = 5.25 to 4.75 V, VD = 5.25 to 3.14 V, VLS = VLC = 5.25 to 1.71 V and T_A = -40° to +85° C. Full-scale input sine wave. Measurement Bandwidth is 10 Hz to 20 kHz.

Parameter		Symbol	Min	Typ	Max	Unit
Single-Speed Mode Fs = 48 kHz						
Dynamic Range	A-weighted		106	114	-	dB
	unweighted		103	111		
Total Harmonic Distortion + Noise	-1 dB			-105	-97	
referred to typical full scale	-20 dB	THD+N	-	-91	-	dB
	-60 dB			-51	-45	
Double-Speed Mode Fs = 96 kHz						
Dynamic Range	A-weighted		106	114		
	unweighted		103	111	-	dB
	40 kHz bandwidth unweighted		-	108		
Total Harmonic Distortion + Noise	-1 dB			-105	-97	
referred to typical full scale	-20 dB			-91	-	
	-60 dB	THD+N	-	-51	-45	dB
	40 kHz bandwidth -1 dB			-102	-	
Quad-Speed Mode Fs = 192 kHz						
Dynamic Range	A-weighted		106	114		
	unweighted		103	111	-	dB
	40 kHz bandwidth unweighted		-	108		
Total Harmonic Distortion + Noise	-1 dB			-105	-97	
referred to typical full scale	-20 dB			-91	-	
	-60 dB	THD+N	-	-51	-45	dB
	40 kHz bandwidth -1 dB			-102	-	
Dynamic Performance for All Modes						
Interchannel Isolation			-	110	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Error			-7	-	7	%
Gain Drift			-	± 100	-	ppm/°C
Offset Error	HPF enabled		0	-	-	LSB
	HPF disabled		-	-	100	
Analog Input Characteristics						
Full-scale Input Voltage			1.02*VA	1.13*VA	1.24*VA	Vpp
Input Impedance (Differential)				250	-	kΩ
Common Mode Rejection Ratio		CMRR	-	82	-	dB

DIGITAL FILTER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Single-Speed Mode (2 kHz to 54 kHz sample rates)					
Passband (Note 1) (-0.1 dB)		0	-	0.47	Fs
Passband Ripple		-0.035		0.035	dB
Stopband (Note 1)		0.58		-	Fs
Stopband Attenuation		-95			dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	12/Fs		s
Double-Speed Mode (54 kHz to 108 kHz sample rates)					
Passband (Note 1) (-0.1 dB)		0	-	0.45	Fs
Passband Ripple		-0.035		0.035	dB
Stopband (Note 1)		0.68		-	Fs
Stopband Attenuation		-92			dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	9/Fs		s
Quad-Speed Mode (108 kHz to 216 kHz sample rates)					
Passband (Note 1) (-0.1 dB)		0	-	0.24	Fs
Passband Ripple		-0.035		0.035	dB
Stopband (Note 1)		0.78		-	Fs
Stopband Attenuation		-92			dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	5/Fs		s
High-Pass Filter Characteristics					
Frequency Response (Note 2) -3.0 dB -0.13 dB		-	1 20	-	Hz
Phase Deviation (Note 2) @ 20 Hz		-	10	-	Deg
Passband Ripple			-	0	dB
Filter Settling Time			10^5/Fs	-	s

Notes:

1. The filter frequency response scales precisely with Fs.
2. Response shown is for Fs equal to 48 kHz. Filter characteristics scale with Fs.

OVERFLOW TIMEOUT

Logic "0" = GND = 0 V; Logic "1" = VLS; C_L = 30 pF, timing threshold is 50% of VLS.

Parameter	Symbol	Min	Typ	Max	Unit
OVFL time-out on overrange condition Fs = 44.1 kHz Fs = 192 kHz		-	$(2^{17}-1)$/Fs 2972 683	-	ms

SERIAL AUDIO INTERFACE - I²S/LJ TIMING

The serial audio port is a three-pin interface consisting of SCLK, LRCK and SDOUT.
Logic "0" = GND = 0 V; Logic "1" = VLS; C_L = 20 pF, timing threshold is 50% of VLS.

Parameter		Symbol	Min	Typ	Max	Unit
Sample Rates	Single-Speed Mode Double-Speed Mode Quad-Speed Mode	-	2 54 108	-	54 108 216	kHz
Master Mode						
SCLK Frequency		-	64*Fs	-	64*Fs	Hz
SCLK Period	1/(64*216 kHz)	t_{PERIOD}	72.3	-	-	ns
SCLK Duty Cycle (Note 1)	(CLKMODE = 0)(Note 2)	t_{HIGH}	40	50	60	%
	(CLKMODE = 1)(Note 2)	t_{HIGH}	28	33	38	%
LRCK setup	before SCLK rising	t_{SETUP1}	20	-	-	ns
LRCK hold	after SCLK rising	t_{HOLD1}	20			
SDOUT setup	before SCLK rising	t_{SETUP2}	10	-	-	ns
SDOUT hold	after SCLK rising (VLS = 1.8 V)	t_{HOLD2}	20			
	after SCLK rising (VLS = 3.3 V)	t_{HOLD2}	10			
	after SCLK rising (VLS = 5 V)	t_{HOLD2}	5			
Slave Mode						
SCLK Frequency (Note 3)		-	-	64*Fs	-	Hz
SCLK Period	1/(64*216 kHz)	t_{PERIOD}	72.3	-	-	ns
SCLK Duty Cycle		t_{HIGH}	28	-	65	%
LRCK setup	before SCLK rising	t_{SETUP1}	20	-	-	ns
LRCK hold	after SCLK rising	t_{HOLD1}	20			
SDOUT setup	before SCLK rising (VLS = 1.8 V)	t_{SETUP2}	4	-	-	ns
	before SCLK rising (VLS = 3.3 V)	t_{SETUP2}	10			
	before SCLK rising (VLS = 5 V)	t_{SETUP2}	10			
SDOUT hold	after SCLK rising (VLS = 1.8 V)	t_{HOLD2}	20			
	after SCLK rising (VLS = 3.3 V)	t_{HOLD2}	10			
	after SCLK rising (VLS = 5 V)	t_{HOLD2}	5			

Notes:

1. Duty cycle of generated SCLK depends on duty cycle of received MCLK as specified under "System Clocking" on page 10.
2. CLKMODE functionality described in Section 4.6.3 "Master Mode Clock Dividers" on page 24.
3. In Slave Mode, the SCLK/LRCK ratio can be set according to preference. However, chip performance is guaranteed only when using the ratios in Section 4.7 Master and Slave Clock Frequencies on page 25.

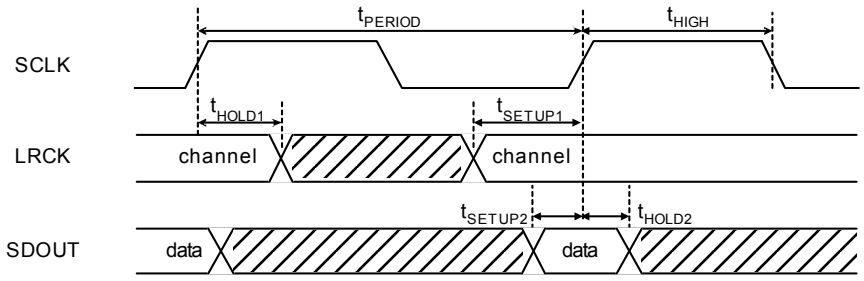


Figure 3. I²S/LJ Timing

SERIAL AUDIO INTERFACE - TDM TIMING

The serial audio port is a three-pin interface consisting of SCLK, LRCK and SDOUT.
Logic "0" = GND = 0 V; Logic "1" = VLS; C_L = 20 pF, timing threshold is 50% of VLS.

Parameter		Symbol	Min	Typ	Max	Unit
Sample Rates	Single-Speed Mode	-	2	-	54	kHz
	Double-Speed Mode	-	54	-	108	kHz
	Quad-Speed Mode[1]	-	108	-	216	kHz
Master Mode						
SCLK Frequency			256*Fs	-	256*Fs	Hz
SCLK Period	1/(256*216 kHz)	t_{PERIOD}	18	-	-	ns
SCLK Duty Cycle (Note 2)	(CLKMODE = 0)(Note 3)	t_{HIGH1}	40	50	60	%
	(CLKMODE = 1)(Note 3)	t_{HIGH1}	28	33	38	%
FS setup	before SCLK rising (Single-Speed Mode)	t_{SETUP1}	20	-	-	ns
FS setup	before SCLK rising (Double-Speed Mode)	t_{SETUP1}	18	-	-	ns
FS setup	before SCLK rising (Quad-Speed Mode)	t_{SETUP1}	5	-	-	ns
FS width	in SCLK cycles	t_{HIGH2}	128	-	128	-
SDOUT setup	before SCLK rising	t_{SETUP2}	5	-	-	ns
SDOUT hold	after SCLK rising	t_{HOLD2}	5	-	-	ns
Slave Mode						
SCLK Frequency (Note 4)			-	256*Fs	-	Hz
SCLK Period	1/(256*216 kHz)	t_{PERIOD}	18	-	-	ns
SCLK Duty Cycle		t_{HIGH1}	28	-	65	%
FS setup	before SCLK rising (Single-Speed Mode)	t_{SETUP1}	20	-	-	ns
FS setup	before SCLK rising (Double-Speed Mode)	t_{SETUP1}	20	-	-	ns
FS setup	before SCLK rising (Quad-Speed Mode)	t_{SETUP1}	10	-	-	ns
FS width	in SCLK cycles	t_{HIGH2}	1	-	244	-
SDOUT setup	before SCLK rising	t_{SETUP2}	5	-	-	ns
SDOUT hold	after SCLK rising	t_{HOLD2}	5	-	-	ns

Notes:

1. TDM Quad-Speed Mode only specified to operate correctly at VLS ≥ 3.14 V.
2. Duty cycle of generated SCLK depends on duty cycle of received MCLK as specified under "System Clocking" on page 10.
3. CLKMODE functionality described in Section 4.6.3 "Master Mode Clock Dividers" on page 24.
4. In Slave Mode, the SCLK/LRCK ratio can be set according to preference; chip performance is guaranteed only when using the ratios in Section 4.7 Master and Slave Clock Frequencies on page 25.

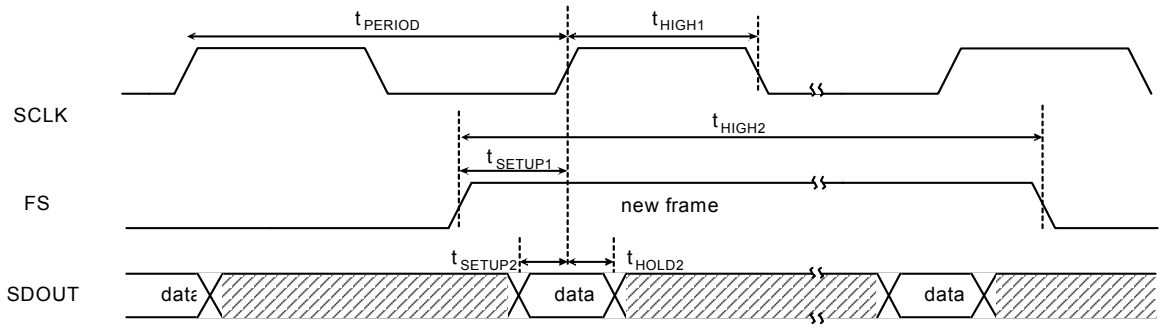


Figure 4. TDM Timing

SWITCHING SPECIFICATIONS - CONTROL PORT - I²C TIMING

Inputs: Logic 0 = DGND, Logic 1 = VLC, SDA C_L = 30 pF

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{\text{RST}}$ Rising Edge to Start	t_{irs}	600	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 1)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising (Note 2)	t_{sud}	600	-	ns
Rise Time of SCL and SDA	t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

Notes:

1. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

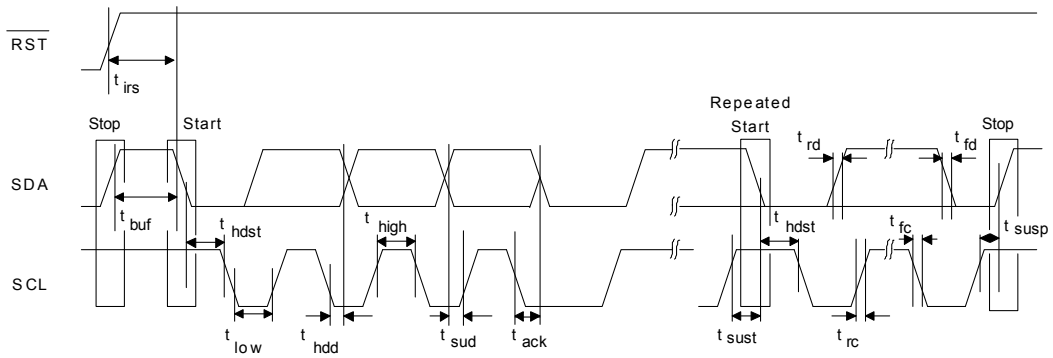


Figure 5. I²C Timing

2. The operational timing specification deviates from the *I2C-Bus Specification and User Manual* of 250 ns.

SWITCHING SPECIFICATIONS - CONTROL PORT - SPI TIMING

Inputs: Logic 0 = DGND, Logic 1 = VLC, CDOUT C_L = 30 pF

Parameter		Symbol	Min	Max	Units
CCLK Clock Frequency		f_{sck}	0	6.0	MHz
$\overline{RST}$ Rising Edge to $\overline{CS}$ Falling		t_{srs}	20		ns
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20		
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0		µs
CCLK Low Time		t_{scl}	66	-	
CCLK High Time		t_{sch}	66		
CDIN to CCLK Rising Setup Time		t_{dsu}	40		
CCLK Rising to DATA Hold Time	(Note 1)	t_{dh}	15		
CCLK Falling to CDOUT Stable		t_{pd}		50	ns
Rise Time of CDOUT		t_{r1}		25	
Fall Time of CDOUT		t_{f1}	-		
Rise Time of CCLK and CDIN	(Note 2)	t_{r2}		100	
Fall Time of CCLK and CDIN	(Note 2)	t_{f2}			

Notes:

1. Data must be held for sufficient time to bridge the transition time of CCLK.
2. For f_{sck} <1 MHz

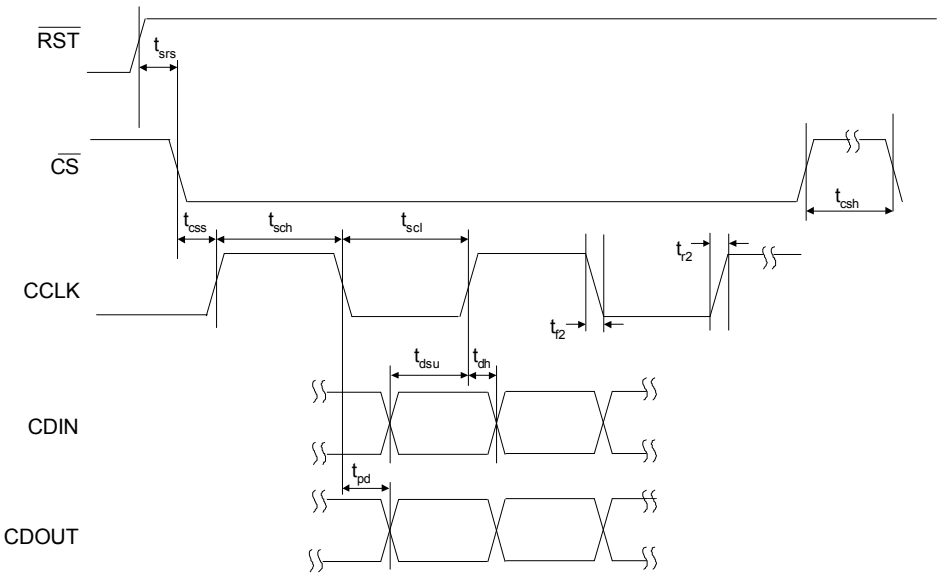


Figure 6. SPI Timing

4. APPLICATIONS

4.1 Power

CS5368 features five independent power pins that power various functional blocks within the device and allow for convenient interfacing to other devices. Table 1 shows what portion of the device is powered from each supply pin. Please refer to "Recommended Operating Conditions" on page 10 for the valid range of each power supply pin. The power supplied to each power pin can be independent of the power supplied to any other pin.

Power Supply Pin		
Pin Name	**Pin Number**	**Functional Block**
VA	4, 9	Analog Core
VX	20	Crystal Oscillator
VD	33	Digital Core
VLS	28	Serial Audio Interface
VLC	35	Control Logic

Table 1. Power Supply Pin Definitions

To meet full performance specifications, the CS5368 requires normal low-noise board layout. The "Typical Connection Diagram" on page 9 shows the recommended power arrangements, with the VA pins connected to a clean supply. VD, which powers the digital filter, may be run from the system logic supply, or it may be powered from the analog supply via a single-pole decoupling filter.

Decoupling capacitors should be placed as near to the ADC as possible, with the lower value high-frequency capacitors placed nearest to the device leads. Clocks should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling of these signals into the device. The FILT+ and VQ decoupling capacitors must be positioned to minimize the electrical path to ground.

The CDB5368 evaluation board demonstrates optimum layout for the device.

4.2 Control Port Mode and Stand-Alone Operation

4.2.1 Stand-Alone Mode

In Stand-Alone Mode, the CS5368 is programmed exclusively with multi-use configuration pins. This mode provides a set of commonly used features, which comprise a subset of the complete set of device features offered in Control Port Mode.

To use the CS5368 in Stand-Alone Mode, the configuration pins must be held in a stable state, at valid logic levels, and $\overline{\text{RST}}$ must be asserted until the power supplies and clocks are stable and valid. More information on the reset function is available in Section 4.5 on page 22.

4.2.2 Control Port Mode

In Control Port Mode, all features of the CS5368 are available. Four multi-use configuration pins become software pins that support the I²C or SPI bus protocol. To initiate Control Port Mode, a controller that supports I²C or SPI must be used to enable the internal register functionality. This is done by setting the CP-EN bit (Bit 7 of the Global Control Port Register). Once CP-EN is set, all of the device configuration pins are ignored, and the internal register settings determine the operating modes of the part. Figure 4.13 on page 30 provides detailed information about the I²C and SPI bus protocols.

4.3 Master Clock Source

The CS5368 requires a Master Clock that can come from one of two sources: an on-chip crystal oscillator driver or an externally generated clock.

4.3.1 On-Chip Crystal Oscillator Driver

When using the on-board crystal oscillator driver, the XTI pin (pin 21) is the input for the Master Clock (MCLK) to the device. The XTO pin (pin 22) must not be used to drive anything other than the oscillator tank circuitry. When using the on-board crystal driver, the topology shown in Figure 7 must be used. The crystal oscillator manufacturer supplies recommended capacitor values. A buffered copy of the XTI input is available as an output on the MCLK pin (pin 23), which is level-controlled by VLS and may be used to synchronize other parts to the device.

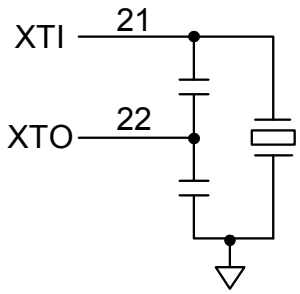


Figure 7. Crystal Oscillator Topology

4.3.2 Externally Generated Master Clock

If an external clock is used, the XTI and XTO pins must be grounded, and the MCLK pin becomes an input for the system master clock. The incoming MCLK should be at the logic level set by the user on the VLS supply pin.

4.4 Master and Slave Operation

CS5368 operation depends on two clocks that are synchronously derived from MCLK: SCLK and LRCK/FS. See Section 4.5 on page 22 for a detailed description of SCLK and LRCK/FS.

The CS5368 can operate as either clock master or clock slave with respect to SCLK and LRCK/FS. In Master Mode, the CS5368 derives SCLK and LRCK/FS synchronously from MCLK and outputs the derived clocks on the SCLK pin (pin 25) and the LRCK/FS pin (pin 24), respectively. In Slave Mode, the SCLK and LRCK/FS are inputs, and the input signals must be synchronously derived from MCLK by a separate device such as another CS5368 or a microcontroller. Figure 8 illustrates the clock flow of SCLK and LRCK/FS in both Master and Slave Modes.

The Master/Slave operation is controlled through the settings of M1 and M0 pins in Stand-Alone Mode or by the M[1] and M[0] bits in the Global Mode Control Register in Control Port Mode. See Section 4.6 on page 23 for more information regarding the configuration of M1 and M0 pins or M[1] and M[0] bits.

Figure 8. Master/Slave Clock Flow

4.4.1 Synchronization of Multiple Devices

To ensure synchronous sampling in applications where multiple ADCs are used, the MCLK and LRCK must be the same for all CS5368 devices in the system. If only one master clock source is needed, one solution is to place one CS5368 in Master Mode, and slave all of the other devices to the one master, as illustrated in Figure 9. If multiple master clock sources are needed, one solution is to supply all clocks from the same external source and time the CS5368 reset de-assertion with the falling edge of MCLK. This will ensure that all converters begin sampling on the same clock edge.

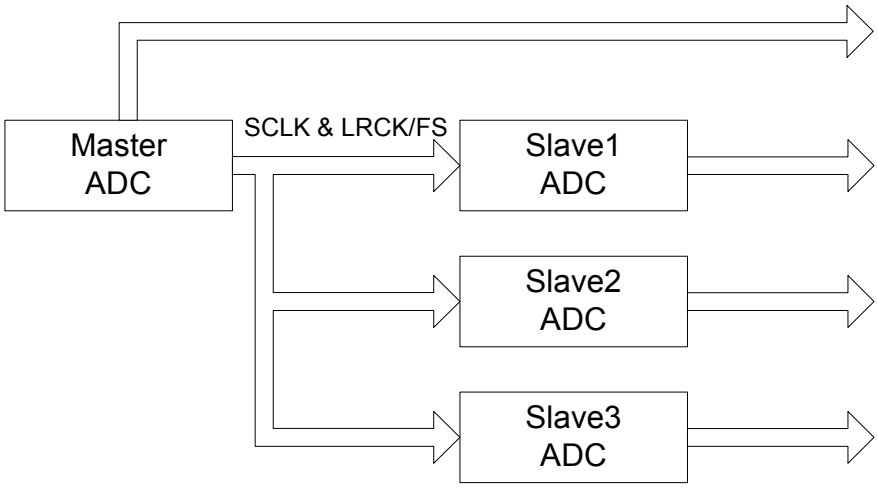


Figure 9. Master and Slave Clocking for a Multi-Channel Application

4.5 Serial Audio Interface (SAI) Format

The SAI port consists of two timing pins (SCLK, LRCK/FS) and four audio data output pins (SDOUT1/TDM, SDOUT2, SDOUT3/TDM and SDOUT4). The CS5368 output is serial data in I²S, Left-Justified (LJ), or Time Division Multiplexed (TDM) digital audio interface formats. These formats are available to the user in both Stand-Alone Mode and Control Port Mode.

4.5.1 I²S and LJ Format

The I²S and LJ formats are both two-channel protocols. During one LRCK period, two channels of data are transmitted, odd channels first, then even. The MSB is always clocked out first.

In Slave Mode, the number of SCLK cycles per channel is fixed as described under "Serial Audio Interface - I²S/LJ Timing" on page 15. In Slave Mode, if more than 32 SCLK cycles per channel are received from a master controller, the CS5368 will fill the longer frame with trailing zeros. If fewer than 24 SCLK cycles per channel are received from a master, the CS5368 will truncate the serial data output to the number of SCLK cycles received. For a complete overview of serial audio interface formats, please refer to Cirrus Logic Application Note AN282.

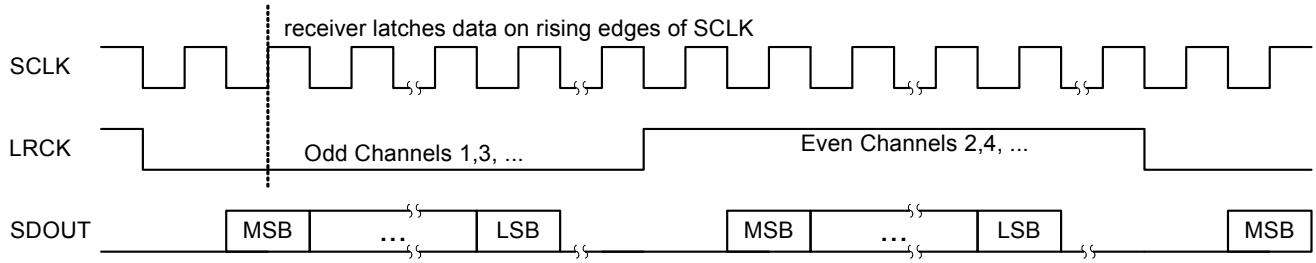


Figure 10. I²S Format

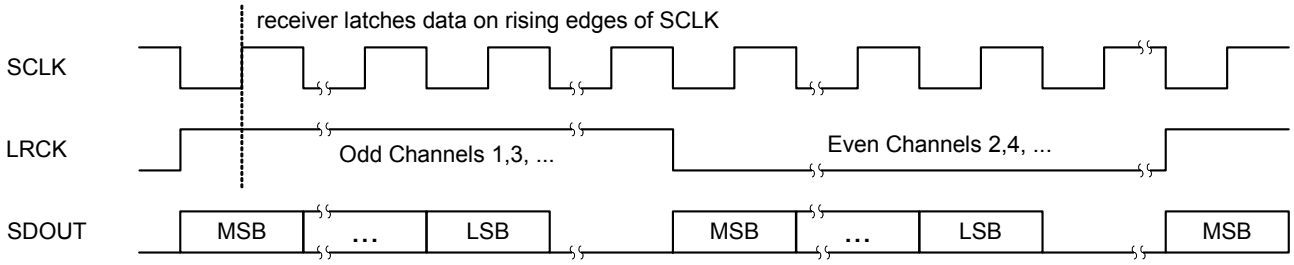


Figure 11. LJ Format

4.5.2 TDM Format

In TDM Mode, all eight channels of audio data are serially clocked out during a single Frame Sync (FS) cycle, as shown in Figure 12. The rising edge of FS signifies the start of a new TDM frame cycle. Each channel slot occupies 32 SCLK cycles, with the data left justified and with MSB first. TDM output data should be latched on the rising edge of SCLK within time specified under "Serial Audio Interface - TDM Timing" section on page 16. The TDM data output port resides on the SDOUT1 pin. The $\overline{\text{TDM}}$ output pin is complimentary TDM data. All SDOUT pins will remain active during TDM Mode. Refer to Section 4.11 "Optimizing Performance in TDM Mode" on page 29 for critical system design information.

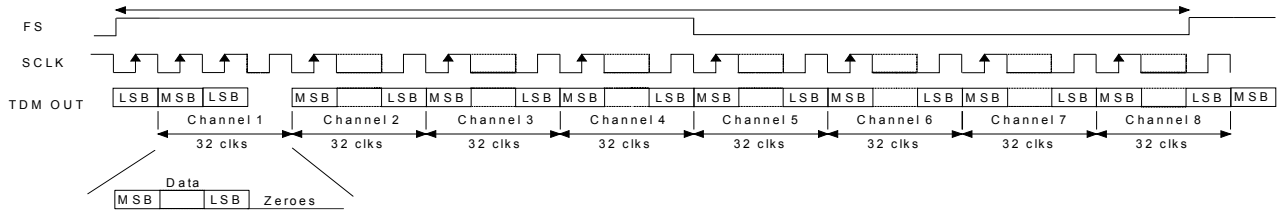


Figure 12. TDM Format

4.5.3 Configuring Serial Audio Interface Format

The serial audio interface format of the data is controlled by the configuration of the DIF1 and DIF0 pins in Stand-Alone Mode or by the DIF[1] and DIF[0] bits in the Global Mode Control Register in Control Port Mode, as shown in Table 2.

DIF1	DIF0	Mode
0	0	Left-Justified
0	1	I²S
1	0	TDM
1	1	Reserved

Table 2. DIF1 and DIF0 Pin Settings

4.6 Speed Modes

4.6.1 Sample Rate Ranges

CS5368 supports sampling rates from 2 kHz to 21 kHz, divided into three ranges: 2 kHz - 54 kHz, 54 kHz - 108 kHz, and 108 kHz - 216 kHz. These sampling speed modes are called Single-Speed Mode (SSM), Double-Speed Mode (DSM), and Quad-Speed Mode (QSM), respectively.

4.6.2 Using M1 and M0 to Set Sampling Parameters

The Master/Slave operation and the sample rate range are controlled through the settings of the M1 and M0 pins in Stand-Alone Mode, or by the M[1] and M[0] bits in the Global Mode Control Register in Control Port Mode, as shown in Table 3.

M1	M0	Mode	Frequency Range
0	0	Single-Speed Master Mode (SSM)	2 kHz - 54 kHz
0	1	Double-Speed Master Mode (DSM)	54 kHz - 108 kHz
1	0	Quadruple-Speed Master Mode (QSM)	108 kHz - 216 kHz
1	1	Auto-Detected Speed Slave Mode	2 kHz - 216 kHz

Table 3. M1 and M0 Settings

4.6.3 Master Mode Clock Dividers

Figure 13 shows the configuration of the MCLK dividers and the sample rate dividers for Master Mode, including the significance of each MCLK divider pin (in Stand-Alone Mode) or bit (in Control Port Mode).

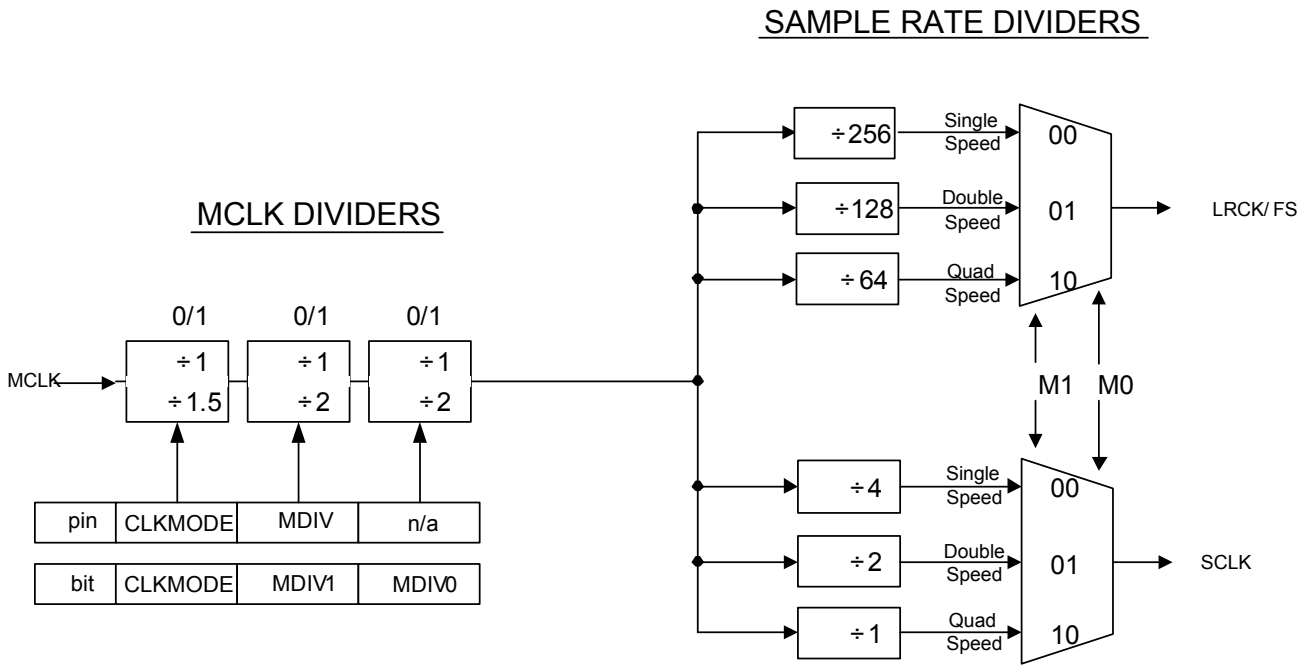


Figure 13. Master Mode Clock Dividers

4.6.4 Slave Mode Audio Clocking With Auto-Detect

In Slave Mode, CS5368 auto-detects speed mode, which eliminates the need to configure M1 and M0 when changing among speed modes. The external MCLK is subject to clock dividers as set by the clock divider pins in Stand-Alone Mode or the clock divider bits in Control Port Mode. The CS5368 compares the divided-down, internal MCLK to the incoming LRCK/FS and sets the speed mode based on the MCLK/LRCK ratio as shown in Figure 14.

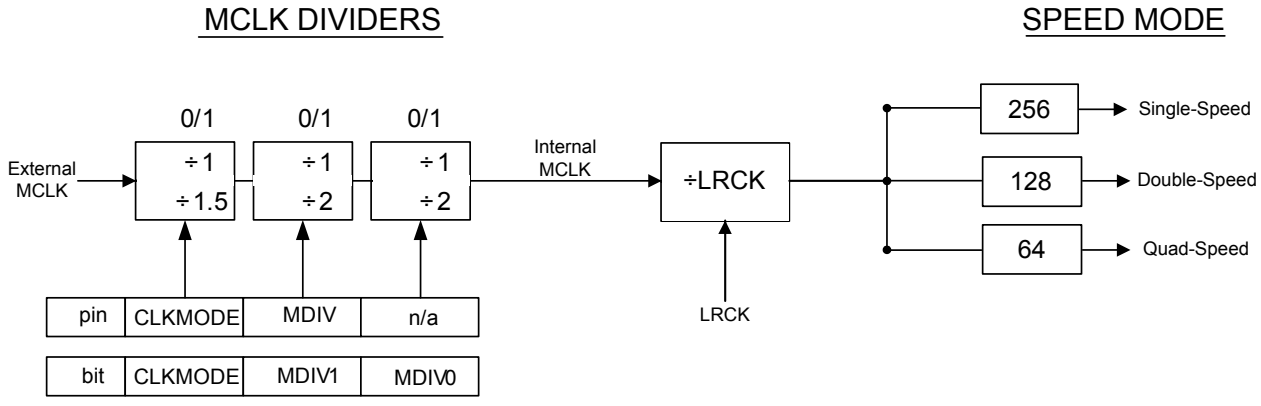


Figure 14. Slave Mode Auto-Detect Speed

4.7 Master and Slave Clock Frequencies

Tables 4 through 12 show the clock speeds for sample rates of 48 kHz, 96 kHz and 192 kHz. The MCLK/LRCK ratio should be kept at a constant value during each mode. In Master Mode, the device outputs the frequencies shown. In Slave Mode, the SCLK/LRCK ratio can be set according to design preference. However, device performance is guaranteed only when using the ratios shown in the tables.

Control Port Mode only

LJ/I²S MASTER OR SLAVE	SSM Fs = 48 kHz				
MCLK Divider	÷**4**	÷3	÷2	÷1.5	÷1
MCLK (MHz)	49.152	36.864	24.576	18.384	12.288
SCLK (MHz)	3.072	3.072	3.072	3.072	3.072
MCLK/LRCK Ratio	1024	768	512	384	256
SCLK/LRCK Ratio	64	64	64	64	64

Table 4. Frequencies for 48 kHz Sample Rate using LJ/I²S

LJ/I²S MASTER OR SLAVE	DSM Fs = 96 kHz				
MCLK Divider	÷**4**	÷3	÷2	÷1.5	÷1
MCLK (MHz)	49.152	36.864	24.567	18.384	12.288
SCLK (MHz)	6.144	6.144	6.144	6.144	6.144
MCLK/LRCK Ratio	512	384	256	192	128
SCLK/LRCK Ratio	64	64	64	64	64

Table 5. Frequencies for 96 kHz Sample Rate using LJ/I²S

LJ/I²S MASTER OR SLAVE	QSM Fs = 192 kHz				
MCLK Divider	÷**4**	÷3	÷2	÷1.5	÷1
MCLK (MHz)	49.152	36.864	24	18.384	12.288
SCLK (MHz)	12.288	12.288	12.288	12.288	12.288
MCLK/LRCK Ratio	256	192	128	96	64
SCLK/LRCK Ratio	64	64	64	64	64

Table 6. Frequencies for 192 kHz Sample Rate using LJ/I²S

TDM MASTER	SSM Fs = 48 kHz				
MCLK Divider	÷**4**	÷3	÷2	÷1.5	÷1
MCLK (MHz)	49.152	36.864	24.567	18.384	12.288
SCLK (MHz)	12.288	12.288	12.288	12.288	12.288
MCLK/FS Ratio	1024	768	512	384	256
SCLK/FS Ratio	256	256	256	256	256

Table 7. Frequencies for 48 kHz Sample Rate using TDM

TDM SLAVE	SSM Fs = 48 kHz				
MCLK Divider	÷**4**	÷3	÷2	÷1.5	÷1
MCLK (MHz)	49.152	36.864	24.567	18.384	12.288
SCLK (MHz)	12.288	12.288	12.288	12.288	12.288
MCLK/FS Ratio	1024	768	512	384	256
SCLK/FS Ratio	256	256	256	256	256

Table 8. Frequencies for 48 kHz Sample Rate using TDM

TDM MASTER	DSM Fs = 96 kHz				
MCLK Divider	÷**4**	÷3	÷2	-	-
MCLK (MHz)	49.152	36.864	24.567	-	-
SCLK (MHz)	24.576	24.576	24.576	-	-
MCLK/FS Ratio	512	384	256	-	-
SCLK/FS Ratio	256	256	256	-	-

Table 9. Frequencies for 96 kHz Sample Rate using TDM

TDM SLAVE	DSM Fs = 96 kHz				
MCLK Divider	÷**4**	÷3	÷2	÷1.5	÷1
MCLK (MHz)	49.152	36.864	24.567	18.384	12.288
SCLK (MHz)	24.576	24.576	24.576	24.576	24.576
MCLK/FS Ratio	512	384	256	192	128
SCLK/FS Ratio	256	256	256	256	256

Table 10. Frequencies for 96 kHz Sample Rate using TDM

TDM MASTER	QSM Fs = 192 kHz				
MCLK Divider	÷**4**	-	-	-	-
MCLK (MHz)	49.152	-	-	-	-
SCLK (MHz)	49.152	-	-	-	-
MCLK/FS Ratio	256	-	-	-	-
SCLK/FS Ratio	256	-	-	-	-

Table 11. Frequencies for 192 kHz Sample Rate using TDM

TDM SLAVE	QSM Fs = 192 kHz				
MCLK Divider	÷**4**	÷3	÷2	÷1.5	÷1
MCLK (MHz)	49.152	36.864	24.567	18.384	12.288
SCLK (MHz)	49.152	49.152	49.152	49.152	49.152
MCLK/FS Ratio	256	192	128	96	64
SCLK/FS Ratio	256	256	256	256	256

Table 12. Frequencies for 192 kHz Sample Rate using TDM

4.8 Reset

The device should be held in reset until power is applied and all incoming clocks are stable and valid. Upon de-assertion of RST, the state of the configuration pins is latched, the state machine begins, and the device starts sending audio output data a maximum of 524288 MCLK cycles after the release of RST. When changing between mode configurations in Stand-Alone Mode, including clock dividers, serial audio interface format, master/slave, or speed modes, it is recommended to reset the device following the change by holding the RST pin low for a minimum of one MCLK cycle and then restoring the pin to a logic-high condition.

4.8.1 Power-Down Mode

The CS5368 features a Power-Down Mode in which power is temporarily withheld from the modulators, the crystal oscillator driver, the digital core, and the serial port. The user can access Power-Down Mode by holding the device in reset and holding all clock lines at a static, valid logic level (either logic-high or logic-low). “DC Power” on page 11 shows the power-saving associated with Power-Down Mode.

4.9 Overflow Detection

4.9.1 Overflow in Stand-Alone Mode

The CS5368 includes overflow detection on all input channels. In Stand-Alone Mode, this information is presented as open drain, active low on the OVFL pin. The pin will go to a logical low as soon as an over-range condition in any channel is detected. The data will remain low, then time-out as specified in Section "Overflow Timeout" on page 14. After the time-out, the OVFL pin will return to a logical high if there has not been any other over-range condition detected. Note that an over-range condition on any channel will restart the time-out period.

4.9.2 Overflow in Control Port Mode

In Control Port Mode, the Overflow Status Register interacts with the Overflow Mask Register to provide interrupt capability for each individual channel. See Section 5.4 "02h (OVFL) Overflow Status Register" on page 33 for details on these two registers.

4.10 Analog Connections

The analog modulator samples the input at half of the internal Master Clock frequency, or 6.144 MHz nominally. The digital filter will reject signals within the stopband of the filter. However, there is no rejection of input signals that are at (N X 6.144 MHz) the digital passband frequency, where n=0,1,2.... Refer to Figure 15, which shows the suggested filter that will attenuate any noise energy at 6.144 MHz in addition to providing the optimum source impedance for the modulators. The use of capacitors that have a large voltage coefficient (such as general-purpose ceramics) must be avoided since these can degrade signal linearity. COG capacitors are recommended for this application. For additional configurations, refer to Cirrus Application Note AN241.

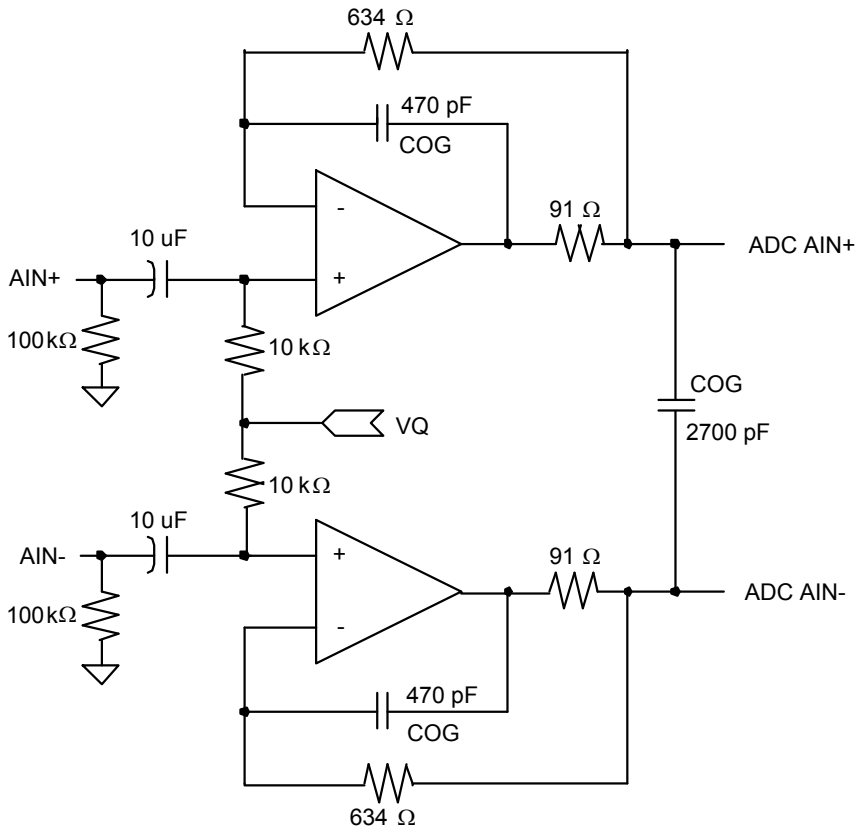


Figure 15. Recommended Analog Input Buffer

4.11 Optimizing Performance in TDM Mode

Noise Management is a design technique that is utilized in the majority of audio A/D converters. Noise management is relatively simple conceptually. The goal of noise management is to interleave the on-chip digital activity with the analog sampling processes to ensure that the noise generated by the digital activity is minimized (ideally non-existant) when the analog sampling occurs. Noise management, when implemented properly, minimizes the on-chip interference between the analog and digital sections of the device. This technique has proven to be very effective and has simplified the process of implementing an A/D converter into a systems design. The dominate source of interference (and most difficult to control) is the activity on the serial audio interface (SAI). However, noise management becomes more difficult to implement as audio sample rates increase simply due to the fact that there is less time between transitions on the SAI.

The CS5368 A/D converter supports a multi-channel Time-Division-Multiplexed interface for Single, Double and Quad-Speed sampling modes. In Single-Speed Mode, sample rates below 50 kHz, the required frequencies of the audio serial ports are sufficiently low that it is possible to implement noise-management. In this mode, the performance of the devices are relatively immune to activity on the audio ports.

However, in Double-Speed and Quad-Speed modes there is insufficient time to implement noise management due to the required frequencies of the audio ports. Therefore, analog performance, both dynamic range and THD+N, can be degraded if the serial port transitions occurr concurrently with the analog sampling. The magnitude of the interference is not only related to the timing of the transition but also the di/dt or transient currents associated with the activity on the serial ports. Even though there is insufficient time to properly implement noise management, the interference effects can be minimized by controlling the transient currents required of the serial ports in Double- and Quad-Speed TDM Modes.

In addition to standard mixed-signal design techniques, system performance can be maximized by following several guidelines during design.

- Operate the serial audio port at 3.3 V and not 5 V. The lower serial port voltage lowers transent currents.
- Operate the A/D converter as a system clock Slave. The serial clock and Left/Right clock become high-impedence inputs in this mode and do not generate significant transient currents.
- Place a buffer on the serial data output very near the A/D converter. Minimizing the stray capacitance of the printed circuit board trace and the loading presented by other devices on the serial data line will minimize the transient current.
- Place a resistor, near the converter, beween the A/D serial data output and the buffer. This resistor will reduce the instantaneous switching currents into the capacitive loads on the nets, resulting in a slower edge rate. The value of the resistor should be as high as possible without causing timing problems elsewhere in the system.

4.12 DC Offset Control

The CS5368 includes a dedicated high-pass filter for each channel to remove input DC offset at the system level. A DC level may result in audible “clicks” when switching between devices in a multi-channel system.

In Stand-Alone Mode, all of the high-pass filters remain enabled. In Control Port Mode, the high-pass filters default to enabled, but may be controlled by writing to the $\overline{\text{HPF}}$ register. If any $\overline{\text{HPF}}$ bit is taken low, the respective high-pass filter is enabled, and it continuously subtracts a measure of the DC offset from the output of the decimation filter. If any $\overline{\text{HPF}}$ bit is taken high during device operation, the value of the DC offset register is frozen, and this DC offset will continue to be subtracted from the conversion result.

4.13 Control Port Operation

The Control Port is used to read and write the internal device registers. It supports two industry standard formats, I²C and SPI. The part is in I²C format by default. SPI Mode is selected if there is ever a high-to-low transition on the AD0/CS pin after the RST pin has been restored high.

In Control Port Mode, all features of the CS5368 are available. Four multi-use configuration pins become software pins that support the I²C or SPI bus protocol. To initiate Control Port Mode, a controller that supports I²C or SPI must be used to enable the internal register functionality. This is done by setting the CP-EN bit (Bit 7 of the Global Control Port Register). Once CP-EN is set, all of the device configuration pins are ignored, and the internal register settings determine the operating modes of the part.

4.13.1 SPI Mode

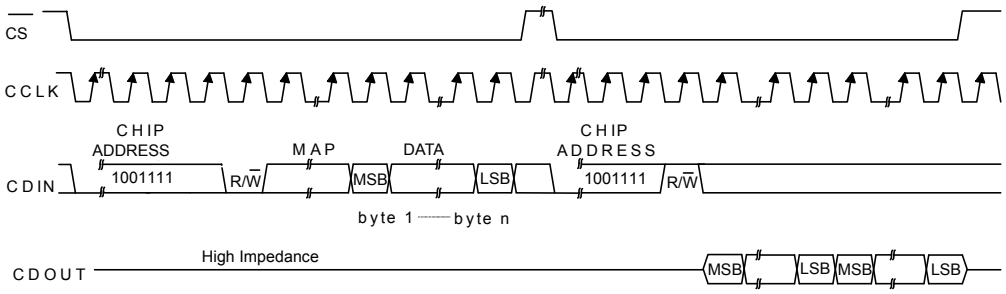
In SPI Mode, CS is the CS5368 chip select signal; CCLK is the control port bit clock (input into the CS5368 from a controller); CDIN is the input data line from a controller; CDOUT is the output data line to a controller. Data is clocked in on the rising edge of CCLK and is supplied on the falling edge of CCLK.

To write to a register, bring CS low. The first seven bits on CDIN form the chip address and must be 1001111. The eighth bit is a read/write indicator (R/W), which should be low to write. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data that will be placed into the register designated by the MAP. During writes, the CDOUT output stays in the Hi-Z state. It may be externally pulled high or low with a 47 kΩ resistor, if desired.

There is a MAP auto-increment capability, which is enabled by the INCR bit in the MAP register. If INCR is a zero, the MAP will stay constant for successive read or writes. If INCR is set to a 1, the MAP will auto-increment after each byte is read or written, allowing block reads or writes of successive registers.

To read a register, the MAP has to be set to the correct address by executing a partial write cycle that finishes (CS high) immediately after the MAP byte. The MAP auto-increment bit (INCR) may be set or not, as desired. To begin a read, bring CS low, send out the chip address and set the read/write bit (R/W) high. The next falling edge of CCLK will clock out the MSB of the addressed register (CDOUT will leave the high impedance state). If the MAP auto-increment bit is set to 1, the data for successive registers will appear consecutively

.



MAP = Memory Address Pointer, 8 bits, MSB first

Figure 16. SPI Format

4.13.2 I²C Mode

In I²C Mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. There is no CS pin. Pins AD0 and AD1 form the two least-significant bits of the chip address and should be connected through a resistor to VLC or DGND, as desired. The state of the pins is latched when the CS5368 is being released from RST.

A Start condition is defined as a falling transition of SDA while SCL is high. A Stop condition is a rising transition of SDA while SCL is high. All other transitions of SDA occur while SCL is low. The first byte sent to the CS5368 after a Start condition consists of a 7-bit chip address field and a R/W bit (high for a read, low for a write). The upper five bits of the 7-bit address field are fixed at 10011. To communicate with a CS5368, the chip address field, which is the first byte sent to the CS5368, should match 10011 and be followed by the settings of the AD1 and AD0. The eighth bit of the address is the R/W bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP), which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto-increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS5368 after each input byte is read and is input to the CS5368 from the microcontroller after each transmitted byte.

Since the read operation cannot set the MAP, an aborted write operation is used as a preamble. The write operation is aborted after the acknowledge for the MAP byte by sending a Stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send start condition.
Send 10011xx0 (chip address & write operation).
Receive acknowledge bit.
Send MAP byte, auto increment off.
Receive acknowledge bit.
Send stop condition, aborting write.
Send start condition.
Send 10011xx1 (chip address & read operation).
Receive acknowledge bit.
Receive byte, contents of selected register.
Send acknowledge bit.
Send stop condition.

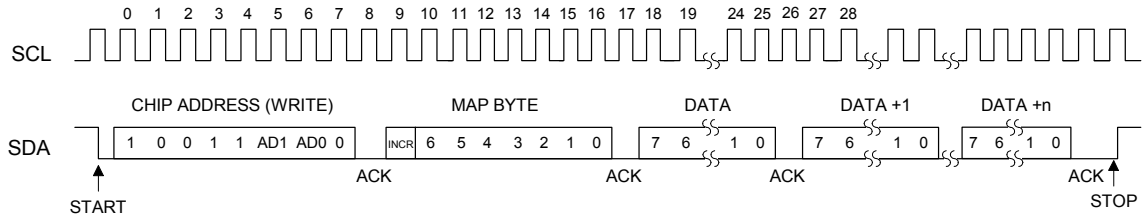


Figure 17. I²C Write Format

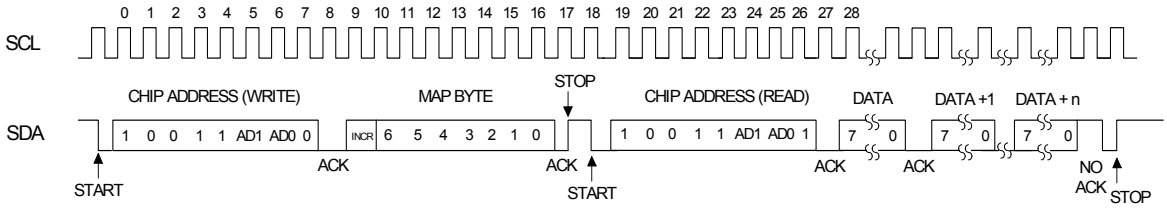


Figure 18. I²C Read Format

5. REGISTER MAP

In Control Port Mode, the bits in these registers are used to control all of the programmable features of the ADC. All registers above 0Ah are RESERVED.

5.1 Register Quick Reference

Adr	Name	7	6	5	4	3	2	1	0
00	REVI	CHIP-ID[3:0]				REVISION[3:0]			
01	GCTL	CP-EN	CLKMODE	MDIV[1:0]		DIF[1:0]		MODE[1:0]	
02	OVFL	$\overline{\text{OVFL8}}$	$\overline{\text{OVFL7}}$	$\overline{\text{OVFL6}}$	$\overline{\text{OVFL5}}$	$\overline{\text{OVFL4}}$	$\overline{\text{OVFL3}}$	$\overline{\text{OVFL2}}$	$\overline{\text{OVFL1}}$
03	OVFM	OVFM8	OVFM7	OVFM6	OVFM5	OVFM4	OVFM3	OVFM2	OVFM1
04	HPF	$\overline{\text{HPF8}}$	$\overline{\text{HPF7}}$	$\overline{\text{HPF6}}$	$\overline{\text{HPF5}}$	$\overline{\text{HPF4}}$	$\overline{\text{HPF3}}$	$\overline{\text{HPF2}}$	$\overline{\text{HPF1}}$
05	RESERVED	-	-	-	-	-	-	-	-
06	PDNE	RESERVED		PDN-BG	PDN-OSC	PDN87	PDN65	PDN43	PDN21
07	RESERVED	-	-	-	-	-	-	-	-
08	MUTE	MUTE8	MUTE7	MUTE6	MUTE5	MUTE4	MUTE3	MUTE2	MUTE1
09	RESERVED	-	-	-	-	-	-	-	-
0A	SDEN	RESERVED				$\overline{\text{SDEN4}}$	$\overline{\text{SDEN3}}$	$\overline{\text{SDEN2}}$	$\overline{\text{SDEN1}}$

5.2 00h (REVI) Chip ID Code & Revision Register

R/W	7	6	5	4	3	2	1	0
R	CHIP-ID[3:0]				REVISION[3:0]			

Default: See description

The Chip ID Code & Revision Register is used to store the ID and revision of the chip.

Bits[7:4] contain the chip ID, where the CS5368 is represented with a value of 0x8.

Bits[3:0] contain the revision of the chip, where revision A is represented as 0x0, revision B is represented as 0x1, etc.

5.3 01h (GCTL) Global Mode Control Register

R/W	7	6	5	4	3	2	1	0
R/W	CP-EN	CLKMODE	MDIV[1:0]		DIF[1:0]		MODE[1:0]	

Default: 0x00

The Global Mode Control Register is used to control the Master/Slave Speed modes, the serial audio data format and the Master clock dividers for all channels. It also contains a Control Port enable bit.

Bit[7] CP-EN manages the Control Port Mode. Until this bit is asserted, all pins behave as if in Stand-Alone Mode. When this bit is asserted, all pins used in Stand-Alone Mode are ignored, and the corresponding register values become functional.

Bit[6] CLKMODE Setting this bit puts the part in 384X mode (divides XTI by 1.5), and clearing the bit invokes 256X mode (divide XTI by 1.0 - pass through).

Bits[5:4] MDIV[1:0] Each bit selects an XTI divider. When either bit is low, an XTI divide-by-1 function is selected. When either bit is HIGH, an XTI divide-by-2 function is selected. With both bits HIGH, XTI is divided by 4.

The table below shows the composite XTI division using both CLKMODE and MDIV[1:0].

CLKMODE,MDIV[1],MDIV[0]	DESCRIPTION
000	Divide-by-1
100	Divide-by-1.5
001 or 010	Divide-by-2
101 or 110	Divide-by-3
011	Divide-by-4
111	Reserved

Bits[3:2] DIF[1:0] Determine which data format the serial audio interface is using to clock-out data.

DIF[1:0]
0x00 Left-Justified format
0x01 I²S format
0x02 TDM
0x03 Reserved

Bits[1:0] MODE[1:0] This bit field determines the device sample rate range and whether it is operating as an audio clocking Master or Slave.

MODE[1:0]
0x00 Single-Speed Mode Master
0x01 Double-Speed Mode Master
0x02 Quad-Speed Mode Master
0x03 Slave Mode all speeds

5.4 02h ($\overline{\text{OVFL}}$) Overflow Status Register

R/W	7	6	5	4	3	2	1	0
R	$\overline{\text{OVFL8}}$	$\overline{\text{OVFL7}}$	$\overline{\text{OVFL6}}$	$\overline{\text{OVFL5}}$	$\overline{\text{OVFL4}}$	$\overline{\text{OVFL3}}$	$\overline{\text{OVFL2}}$	$\overline{\text{OVFL1}}$

Default: 0xFF, no overflows have occurred.

Note: This register interacts with Register 03h, the Overflow Mask Register.

The Overflow Status Register is used to indicate an individual overflow in a channel. If an overflow condition on any channel is detected, the corresponding bit in this register is asserted (low) in addition to the open drain active low $\overline{\text{OVFL}}$ pin going low. Each overflow status bit is sticky and is cleared only when read, providing full interrupt capability.

5.5 03h (OVFM) Overflow Mask Register

R/W	7	6	5	4	3	2	1	0
R/W	OVFM8	OVFM7	OVFM6	OVFM5	OVFM4	OVFM3	OVFM2	OVFM1

Default: 0xFF, all overflow interrupts enabled.

The Overflow Mask Register is used to allow or prevent individual channel overflow events from creating activity on the $\overline{\text{OVFL}}$ pin. When a particular bit is set low in the Mask register, the corresponding overflow bit in the Overflow Status register is prevented from causing any activity on the $\overline{\text{OVFL}}$ pin.

5.6 04h (HPF) High-Pass Filter Register

R/W	7	6	5	4	3	2	1	0
R/W	HPF8	HPF7	HPF6	HPF5	HPF4	HPF3	HPF2	HPF1

Default: 0x00, all high-pass filters enabled.

The High-Pass Filter Register is used to enable or disable a high-pass filter that exists for each channel. These filters are used to perform DC offset calibration, a procedure that is detailed in "DC Offset Control" on page 29.

5.7 05h Reserved

R/W	7	6	5	4	3	2	1	0
RESERVED	-	-	-	-	-	-	-	-

5.8 06h (PDN) Power Down Register

R/W	7	6	5	4	3	2	1	0
R/W	RESERVED		PDN-BG	PDN-OSC	PDN87	PDN65	PDN43	PDN21

Default: 0x00 - everything powered up

The Power Down Register is used as needed to reduce the chip's power consumption.

Bit[7] RESERVED

Bit[6] RESERVED

Bit[5] PDN-BG When set, this bit powers-down the bandgap reference.

Bit[4] PDN-OSC controls power to the internal oscillator core. When asserted, the internal oscillator core is shut down, and no clock is supplied to the chip. If the chip is running off an externally supplied clock at the MCLK pin, it is also prevented from clocking the device internally.

Bit[3:0] PDN When any bit is set, all clocks going to a channel pair are turned off, and the serial data outputs are forced to all zeroes.

5.9 07h Reserved

R/W	7	6	5	4	3	2	1	0
RESERVED	-	-	-	-	-	-	-	-

5.10 08h (MUTE) Mute Control Register

R/W	7	6	5	4	3	2	1	0
R/W	MUTE8	MUTE7	MUTE6	MUTE5	MUTE4	MUTE3	MUTE2	MUTE1

Default: 0x00, no channels are muted.

The Mute Control Register is used to mute or unmute the serial audio data output of individual channels. When a bit is set, that channel's serial data is muted by forcing the output to all zeroes.

5.11 09h Reserved

R/W	7	6	5	4	3	2	1	0
RESERVED	-	-	-	-	-	-	-	-

5.12 0Ah ($\overline{\text{SDEN}}$) SDOUT Enable Control Register

R/W	7	6	5	4	3	2	1	0
R/W	RESERVED				SDEN4	SDEN3	SDEN2	SDEN1

Default: 0x00, all SDOUT pins enabled.

The SDOUT Enable Control Register is used to tri-state the serial audio data output pins. Each bit, when set, tri-states the associated SDOUT pin.

6. FILTER PLOTS

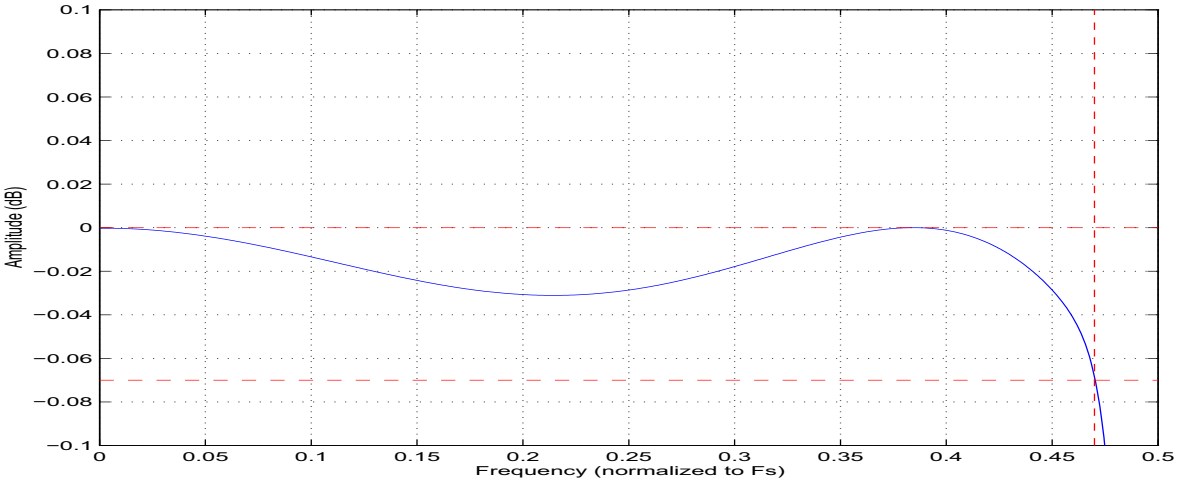


Figure 19. SSM Passband

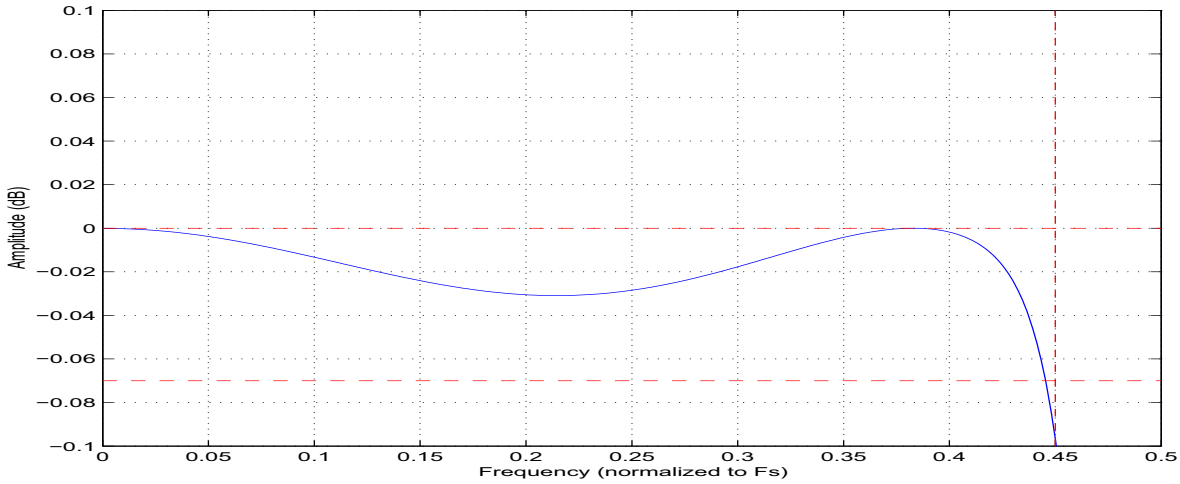


Figure 20. DSM Passband

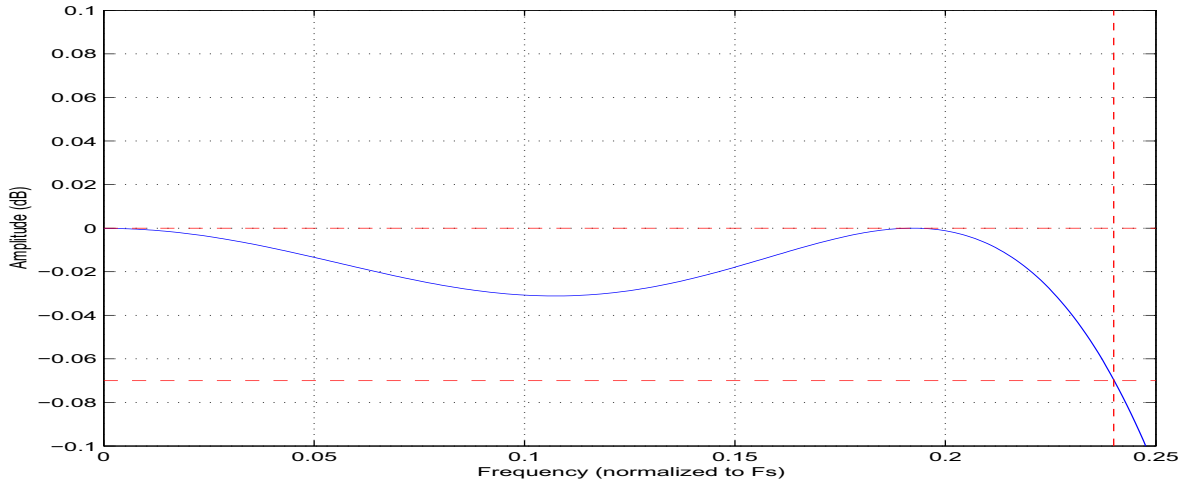


Figure 21. QSM Passband

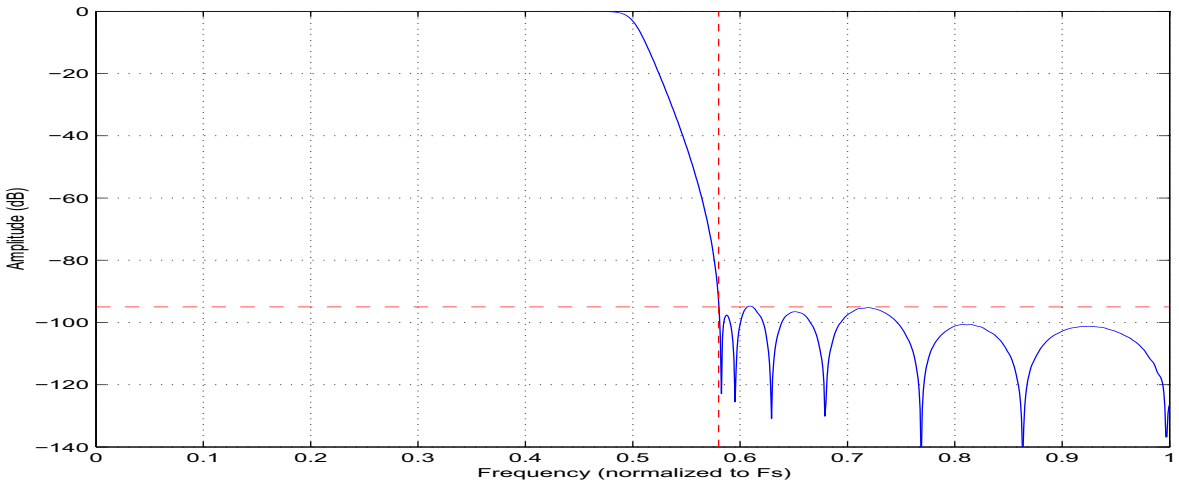


Figure 22. SSM Stopband

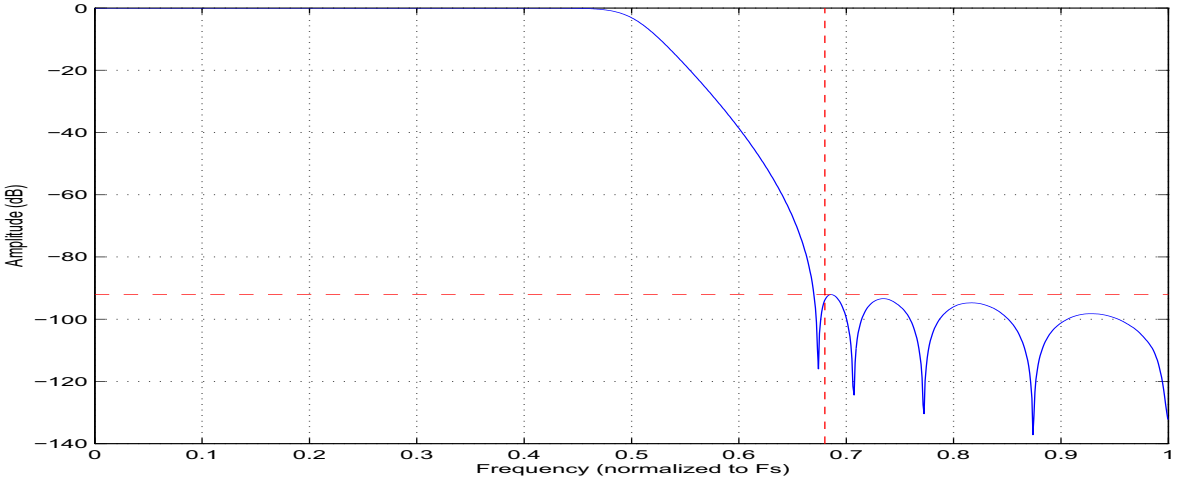


Figure 23. DSM Stopband

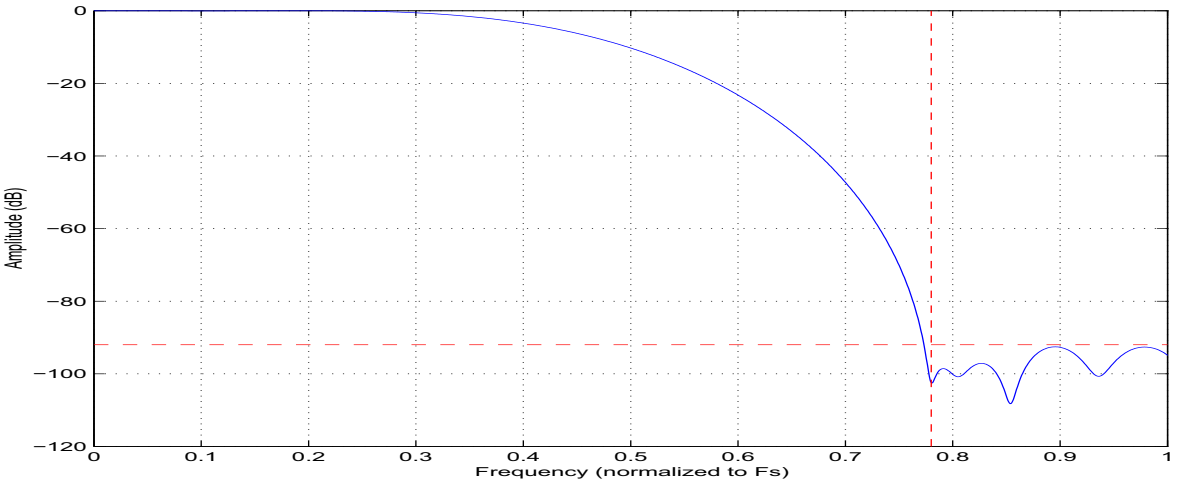


Figure 24. QSM Stopband

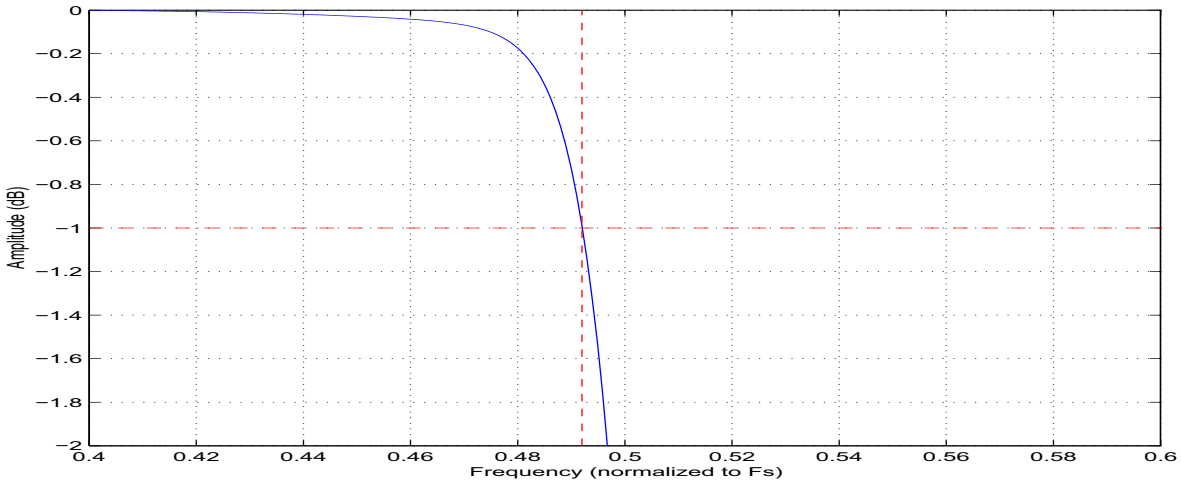


Figure 25. SSM -1 dB Cutoff

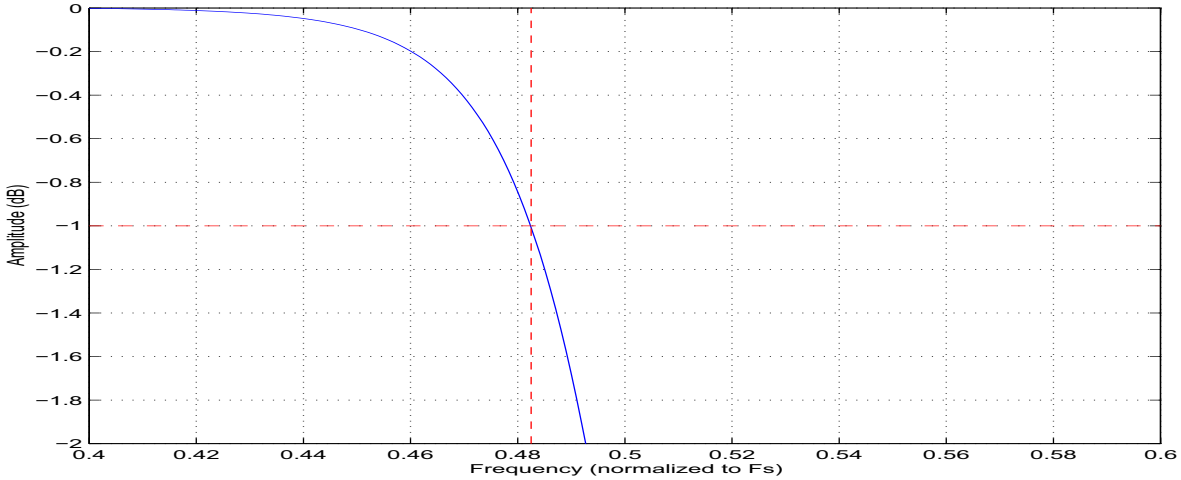


Figure 26. DSM -1 dB Cutoff

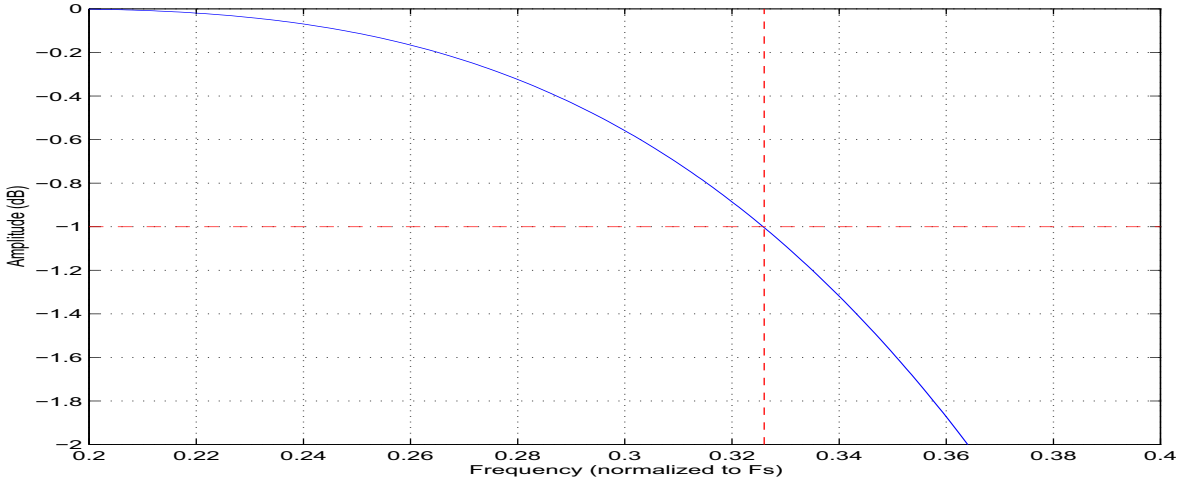


Figure 27. QSM -1 dB Cutoff

7. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-199, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels. The dynamic range is specified with and without an A-weighting filter.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A. Specified using an A-weighting filter.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between one channel and all remaining channels, measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to all other channels. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

Intrachannel Phase Deviation

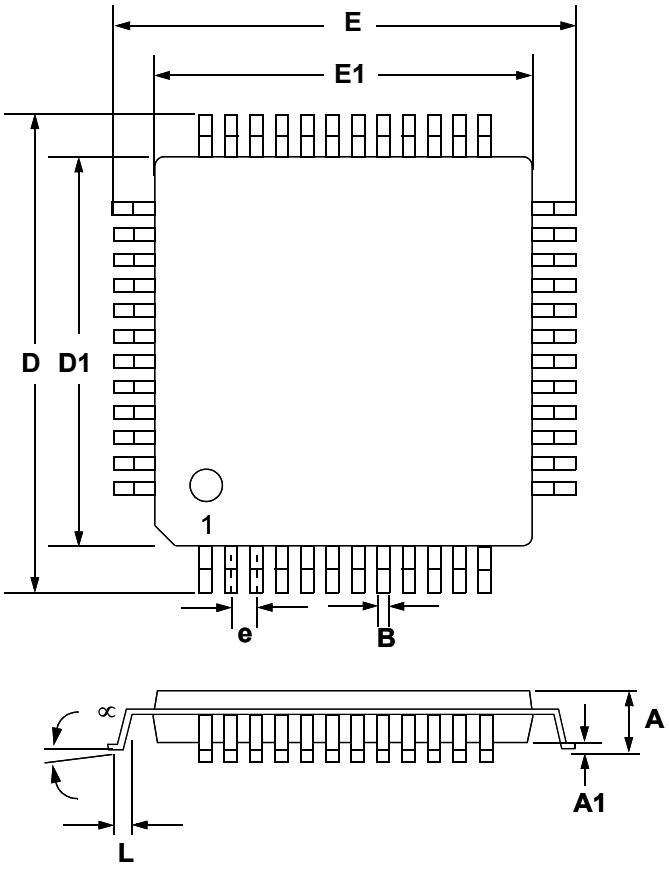
The deviation from linear phase within a given channel.

Interchannel Phase Deviation

The difference in phase response between channels.

8. PACKAGE DIMENSIONS

48L LQFP PACKAGE DRAWING



	INCHES			MILLIMETERS		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	---	0.055	0.063	---	1.40	1.60
A1	0.002	0.004	0.006	0.05	0.10	0.15
B	0.007	0.009	0.011	0.17	0.22	0.27
D	0.343	0.354	0.366	8.70	9.0 BSC	9.30
D1	0.272	0.28	0.280	6.90	7.0 BSC	7.10
E	0.343	0.354	0.366	8.70	9.0 BSC	9.30
E1	0.272	0.28	0.280	6.90	7.0 BSC	7.10
e*	0.016	0.020	0.024	0.40	0.50 BSC	0.60
L	0.018	0.24	0.030	0.45	0.60	0.75
∝	0.000°	4°	7.000°	0.00°	4°	7.00°

* Nominal pin pitch is 0.50 mm
Controlling dimension is mm. JEDEC Designation: MS026

THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Allowable Junction Temperature		-	-	135	°C
Package Thermal Resistance	θ_{JA}	-	48	-	°C/W
	θ_{JC}	-	15	-	

9. ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS5368	114 dB, 192 kHz, 8-channel A/D Converter	48-pin LQFP	YES	Commercial	-40°C to +85°C	Tray	CS5368-CQZ
						Tape & Reel	CS5368-CQZR
				Automotive	-40°C to +105°C	Tray	CS5368-DQZ
						Tape & Reel	CS5368-DQZR
CDB5368	Evaluation Board for CS5368						CDB5368

10.REVISION HISTORY

Revision	Changes
F1 DEC '06	Initial release.
F2 JUL '07	Updated the wording of pin 24, LRCK/FS, in the pin description table on page 7 to correctly reflect the high/low clocking state for odd-channel c in I²S and LJ Modes.
F3 JAN '08	Corrected SCL/CCLK pin description (Pin 39) for "Control Port Mode" on page 8.
F4 APR '09	Corrected Absolute Max temp for "Ambient Operating Temperature (Power Applied)" on page 10.
F5 JUL '14	Updated I^2C and SPI bullet under "Additional Control Port Features" on page 1. Added Note 2 to "Switching Specifications - Control Port - I²C Timing" on page 17.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.